IN THE CLAIMS

Please amend claims 1 and 15 as follows:

1. (Currently Amended) A process variation compensation circuit comprising:

a threshold voltage detector circuit configured with at least one transistor that is manufactured during a process, the threshold voltage detector generating an output signal dependant on variations in the process;

a comparator network coupled to the threshold voltage detector, the comparator network receiving the output signal and generating at least two responsive logic signals that are indicative of the output signal; and

a compensation circuit including first and second logic gates each configured to receive the at least two logic signals and a circuit block coupled to the logic gates and including at least one transistor manufactured from the process, the circuit block configured to receive outputs of the logic gates and to adjust the circuit block according to certain outputs of the logic gates, wherein the circuit block is an inverter and wherein the adjustment to the circuit block includes, dependent on the outputs of the logic gates, adding a transistor to or removing a transistor from the inverter.

2.-4. (Cancelled)

5. (Previously Presented) The circuit of claim 1 wherein the threshold voltage detector comprises a NMOS transistor that is manufactured during the process and wherein the output signal varies according to a threshold voltage of the NMOS transistor; and

wherein the logic gates include an OR gate and an AND gate, and wherein a first transistor is added to the inverter or removed from the inverter dependent on an output of the OR gate and a second transistor is added to the inverter or removed from the inverter dependent on an output of the AND gate.

6. (Original) The circuit of claim 5 wherein the threshold voltage detector circuit is an NMOS threshold voltage detector including the NMOS transistor and a reference current configured between a power supply voltage and ground, and wherein the output signal is a threshold voltage signal of the NMOS threshold voltage detector that varies according to the threshold voltage of the NMOS transistor.

7. (Previously Presented) The circuit of claim 1 wherein the threshold voltage detector circuit comprises a PMOS transistor that is manufactured during the process and wherein the output signal varies according to a threshold voltage of the PMOS transistor; and

wherein the logic gates include a NOR gate and a NAND gate, and wherein a first transistor is added to the inverter or removed from the inverter dependent on an output of the NOR gate and a second transistor is added to the inverter or removed from the inverter dependent on an output of the NAND gate.

8. (Original) The circuit of claim 7 wherein the threshold voltage detector circuit is an PMOS threshold voltage detector including the PMOS transistor and a reference current configured between a power supply voltage and ground, and wherein the output signal is a threshold voltage signal of the PMOS threshold voltage detector that varies according to the threshold voltage of the PMOS transistor.

9. (Original) The circuit of claim 1 wherein the comparator network comprises a high and a low comparator, each having a first and second input and an output, and a voltage reference network, wherein the first input of the low comparator receives a first reference voltage from the voltage reference network, the first input of the high comparator receives a second reference voltage from the voltage reference network, the second input of both the high and low comparators receive the output signal from the threshold voltage detector circuit, and wherein the high and low comparators each generate high and low logic signals representative of a comparison of a reference voltage and the output signal.

10. (Original) The circuit of claim 9 wherein a normal range is established between the first reference voltage and the second reference voltage such that when the output signal is between the first and second reference voltages high and low logic signals indicate that the output signal is in normal range.

11. (Original) The circuit of claim 10 wherein no adjustment is made to the circuit block when the output signal is in the normal range.

12. (Original) The circuit of claim 10 wherein an adjustment is made to the circuit block when the output signal is not in the normal range.

13. (Original) The circuit of claim 1 wherein the circuit block is an inverter and wherein the adjustment to the circuit block includes adding a transistor to the inverter when the logic signals indicate that the threshold detector has detected a low output signal.

14. (Original) The circuit of claim 1 wherein the circuit block is an inverter and wherein the adjustment to the circuit block includes removing a transistor from the inverter when the logic signals indicate that the threshold detector has detected a high output signal.

15. (Currently Amended) A method of compensating for process variation of semiconductors in a circuit comprising:

detecting a threshold voltage of a circuit including at least one semiconductor that is manufactured during a process;

comparing the detected threshold voltage with known voltages;

generating <u>at least two</u> logic signals that are indicative the comparison of the of the threshold voltage with known voltages;

receiving the <u>at least two</u> logic signals by <u>each of first and second</u> logic gates; and

adjusting a circuit block based on outputs of the logic gates, wherein the circuit block includes at least one transistor that is manufactured from the process, wherein the circuit block is

an inverter and wherein the adjustment to the circuit block includes, dependent on the outputs of the logic gates, adding a transistor to or removing a transistor from the inverter.

16. (Cancelled)

17. (Original) The method of claim 15 wherein detecting the threshold voltage of a circuit includes detecting a threshold voltage signal of a circuit including a NMOS transistor that is manufactured during the process and wherein the threshold voltage signal varies according to a threshold voltage of the NMOS transistor.

18. (Original) The method of claim 15 wherein detecting the threshold voltage of a circuit includes detecting a threshold voltage signal of a circuit including a PMOS transistor that is manufactured during the process and wherein the threshold voltage signal varies according to a threshold voltage of the PMOS transistor.

19. (Original) The method of claim 15 wherein a normal range is established between a first known voltage and a second known voltage such that logic signals indicate that the detected threshold voltage is in normal range when the detected threshold voltage is between the first and second known voltages.

20. (Original) The method of claim 19 wherein no adjustment is made to the circuit block when the detected threshold voltage is in the normal range.

21. (Original) The method of claim 19 wherein an adjustment is made to the circuit block when the detected threshold voltage is not in the normal range.

22. (Original) The method of claim 15 wherein adjusting a circuit block includes adding a semiconductor to the circuit block when the logic signals indicate that a low threshold voltage was detected.

23. (Original) The method of claim 15 wherein adjusting a circuit block includes removing a semiconductor to the circuit block when the logic signals indicate that a high threshold voltage was detected.

24. (Previously Presented) The circuit of claim 5 wherein the first transistor and the second transistor are added to the inverter when there is weak NMOS as a result of process effect, the first transistor is added to and the second transistor is removed from the inverter when the process effect has not caused transistors to leave a normal range and the first transistor and the second transistor are removed from the inverter when there is strong NMOS as a result of process effect.

25. (Previously Presented) The circuit of claim 7 wherein the first transistor and the second transistor are added to the inverter when there is strong PMOS as a result of process effect, the first transistor is added to and the second transistor is removed from the inverter when the process effect has not caused transistors to leave a normal range and the first transistor and the second transistor are removed from the inverter when there is weak PMOS as a result of process effect.